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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,301	04/16/2004	Shin Koide	119129	7757

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,301	KOIDE ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/04 & 2/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Priority to Japanese Patent Application No. 2003-139205 (May 16, 2003) is claimed.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,633,359 B1 (to Zhang et al.) in view of United States Patent 6,297,862 B1 (to Murade).

As to claims 1, 8, 11 and 12, Zhang teaches and discloses a liquid crystal display device comprising an active matrix substrate (Figure 1, first substrate 1) having a plurality of scanning lines (Figure 2, scanning lines 15) and a plurality of data lines (Figure 2, signal lines 11) provided such that they intersect each other (See Figure 2), thin film transistors (Figures 1 and 2, TFT 25) provided in association with intersections of data lines (Figure 2, signal lines 11) and scanning lines (Figure 2, scanning lines 15) and pixel electrodes (Figures 1 and 2, pixels 24) connected to the thin film transistors (Figures 1 and 2, TFTs 25), an opposing substrate (Figure 1, second substrate 3) disposed such that it opposes the active matrix substrate (Figure 1, first substrate 1) and a liquid crystal layer (Figure 1, liquid crystal "E") the thin film transistors are formed of P-type transistors having semiconductor layers (Figure 11C, P-type TFTs 75b and polysilicon layers 41a and 41c), a plurality of gate electrodes (identified as "G" in Figure 2) intersecting the semiconductor layers at a plurality of locations and LDD portions in which P-type lightly doped regions are formed at least on one side of channel regions of the semiconductor layers (See Figure 11D for example and Column 13, Lines 25-30).

Zhang does not appear to explicitly specify a light shielding device provided on both sides in a direction of thickness of the thin-film transistors.

Murade teaches and discloses a light shielding structure of a substrate for a liquid crystal device, liquid crystal device and projection type display device and teaches a first light shielding film below the channel region of a TFT and a second light shielding film above the channel region (Abstract, Figure 6, channel region 1c, first light shield film 7 and second light shield film 3).

It would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Zhang in view of Murade to prevent light from entering the channel region and to minimize leakage current generated from a TFT exposed to light (Column 2, Lines 1-10).

Thus, claims 1, 8, 11 and 12 are rejected.

As to claims 2, 3, 9 and 10, (Murade) the second light shielding film (3) of Figure 6 is a data line (Column 13) and it overlaps the channel region (1c) to serve as a light shield.

Thus, claims 2, 3, 9 and 10 are rejected.

As to claim 5, (Murade) the scan line (2) covers the channel region (1c of Figure 6).

Thus, claim 5 is rejected.

As to claim 6, (Murade) the semiconductor layers are at least polysilicon (Column 10, Lines 40-50).

Thus, claim 6 is rejected.

As to claim 7, Murade also teaches a black matrix (Figure 2, black matrix 6) is formed on the opposing substrate at a position corresponding to the channel regions.

Thus, claim 7 is rejected.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,633,359 B1 (to Zhang et al.)(Zhang I) in view of United States Patent 6,297,862 B1 (to Murade) and further in view of United States Patent 5,717,224 (to Zhang)(Zhang II).

As to claim 4, Zhang I does not appear to explicitly specify a reflective layer formed on the active matrix substrate to perform reflective display and a part of the reflective layer formed such that it planarly overlaps the channel regions of the semiconductor layers so as to constitute the light shielding device.

Zhang II teaches and discloses a semiconductor device having an insulated gate field effect thin film transistor and teaches a channel region (Figure 5, channel region 508) and an electrode and wiring line that covers the channel region (Figure 5, gate electrode 504).

It would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Zhang I in view of Zhang II to prevent light from reaching the channel region and to render stable the thin film transistor (Abstract).

Thus, claim 4 is rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio
Patent Examiner
Art Unit 2871

JDG

ANDREW SCHECHTER
PRIMARY EXAMINER